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Ultra Low Power Based TCFF in 40nm CMOS Technology

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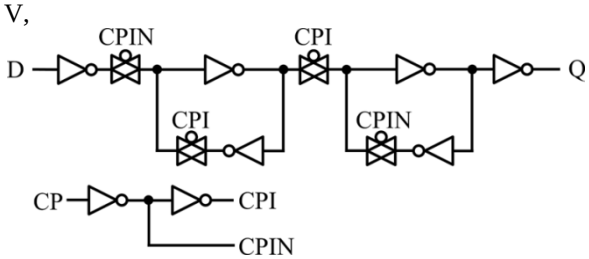
Abstract
An extremely low-power flip-flop (FF) named topologically- compressed flip-flop (TCFF) is proposed. As compared with conventional FFs, the FF reduces power dissipation by 75% at 0% data activity. This power reduction ratio is the highest among FFs that have been reported so far. The reduction is achieved by applying topological compression method, merger of logically equivalent transistors to an unconventional latch structure. The very small number of transistors, only three, connected to clock signal reduces the power drastically, and the smaller total transistor count assures the same cell area as conventional FFs. In addition, fully static full-swing operation makes the cell tolerant of supply voltage and input slew variation. An experimental chip design with 40 nm CMOS technology shows that almost all conventional FFs are replaceable with proposed FF while preserving the same system performance and layout area.

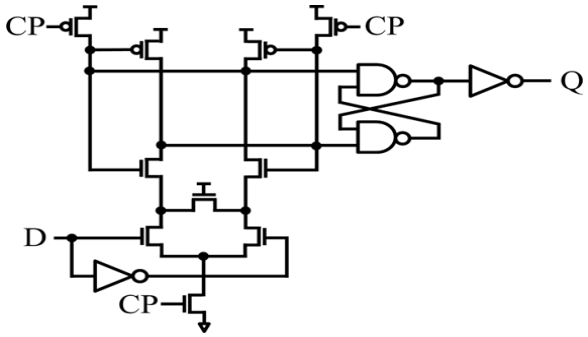
I. INTRODUCTION

The mobile market keeps on expanding. In addition to the conventional mobile phone, digital camera, and tablet PC, development of various kinds of wearable information equipment or healthcare associated equipment has newly prospered in recent years. In those kinds of battery-working equipment, reduction of power is a very important issue, and demand for power reduction in LSI is increasing. Based on such background, various kinds of circuit technique have already been proposed. In LSI, generally more than half of the power is dissipated in random logic of which half of the power is dissipated by flip-flops (FFs). During the past dozen years, several low-power FFs have been rushed into development. However, in actual chip design, the conventional FF is still used most often as a preferred FF because of its well-balanced power, performance and cell area. The purpose of this paper is to present a solution to achieve all of the goals: power reduction without any degradation of timing performance and cell area.

THE versatile business continues growing. Not with standing the routine cellular telephone, advanced cam, and tablet PC, improvement of different sorts of wearable data supplies or human services related gear has recently flourished as of late. In those sorts of battery-working supplies, decrease of force is a critical issue, and interest for force lessening in LSI is expanding. Taking into account such foundation, different sorts of circuit system have as of now been proposed. In LSI, by and large more than 50% of the force is dispersed in irregular rationale, of which 50% of the force is dispersed by flip-flops (FFs). Amid the past dozen years, a few low-control FFs have been raced into advancement. Not with standing, in real chip outline, the customary FF is still utilized frequently as a favored FF in light of its decently adjusted power, execution and cell range. The motivation behind this paper is to present an answer for accomplish the greater part of the objectives: power diminishment with no corruption of timing execution and cell region. In Section II, we survey existing low-control FFs. In Segment III, we demonstrate our configuration approach. In Section IV, we propose FF acknowledgment with another system. In Section V,



1.Conventional transmission-gate flip-flop (TGFF).



2.Differential sense-amplifier flip-flop (Diff FF).

The definite force and execution attributes are indicated contrasted with different FFs. In Section VI, we demonstrate the impact of the proposed FF in real chip outline by test format. At last, in Section VII, we demonstrate the best approach to apply the proposed FF successfully to different frameworks in perspective of force and performance.

II. BACKGROUND

In this segment, we examine issues on beforehand reported average low-control FFs with examination to an ordinary FF indicated in Fig. 1.

Fig. 2 demonstrates an average circuit of differential sense-intensifier sort FF (Diff FF) [1]–[3]. This sort of circuit is extremely powerful to increase little swing signs, so is by and large utilized as a part of yield of memory circuits. In this FF, then again, the impact of force reduction goes down in the state of lower information action, be- cause these sorts of circuits have precharge operation in every clock low state. More over, if we use reduced clock swing, customized clock generator and an additional predisposition circuit are vital.

Fig.3showsacircuitofconditional-clocking type FF(CCFF) [4]–[6]. This circuit is attained to from an utilitarian perspective. The circuit screens data information change in every clock cycle also debilitates the operation of inward clock if data information are not changed. By this operation, force is lessened when data information are not changed. Anyway sadly, its cell zone gets to be pretty much twofold that of the ordinary circuit indicated in Fig1.

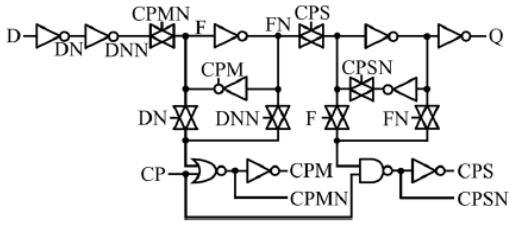


Figure 3: conditional clocking Flip Flop (CCFF)

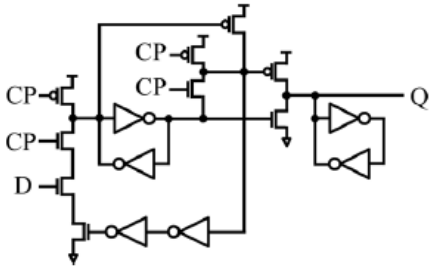


Figure 4: Cross-charge Control Flip-Flop (XCFF)

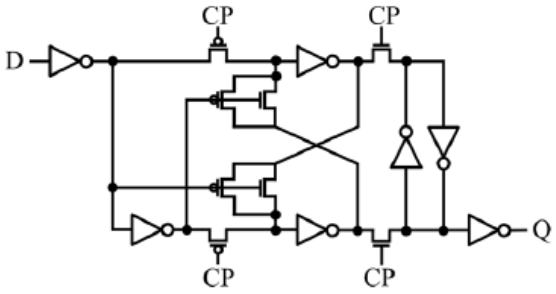


Figure 5: Adaptive- Coupling Flip-Flop (ACFF)

And mainly due to this size issue, it becomes hard to use if the logic area is relatively large in the chip. Fig.4 shows the circuit of cross-charge control FF (XCFF)[7]. The feature of this circuit is to drive output transistors separately in order to reduce charged and discharged gate capacitance. However, in actual operation, some of the internal nodes are pre-set with clock signal in the case of data is high, and this operation dissipates extra power to charge and discharge internal nodes. As a result, the effect of power reduction will decrease. Circuits including pre-set operation have the same problem [8].The adaptive-coupling type FF (ACFF) [9], shown in Fig. 5,is based on a 6-transistor memory cell. In this circuit, instead of the commonly used double-channel transmission-gate, a single-channel transmission-gate with additional dynamic circuit has been used for the data line in order to reduce clock-related transistor count. However, in this circuit, delay is easily affected by input clock slew variation because different types of single channel transmission-gates are used in the same data line and connected to the same clock signal. Moreover, characteristics of single-channel transmission-gate circuits and dynamic circuits are strongly affected by process variation. Thus, their optimization is relatively difficult, and performance degradation across various process corners is a concern. Let us summarize the analysis on previously reported low-power FFs. For Diff FF [1] and XCFF [7], pre-charge operation is a concern especially in lower data activity. As regards CCFF[4], its cell area becomes a bottleneck to use. And for ACFF Fig. 6. Example of combinational type

FF.[9], tolerance for input clock slew variation becomes subject to resolve.

III. DESIGN APPROACH

In order to reduce the power of the FF while keeping competitive performance and similar cell area, we tried to reduce the transistor count, especially those operating with clock signals, without introducing any dynamic or pre-charge circuit. The power of the FF is mostly dissipated in the operation of clock-related transistors, and reduction of transistor count is effective to avoid cell area increase and to reduce load capacitance in internal nodes. In the conventional FF shown in Fig. 1,there are 12 clock-related transistors. To reduce clock-related transistor counts directly from this circuit is quite difficult. One reason is because transmission-gates need a 2-phase clock signal, thus the clock driver cannot be eliminated. Another reason is that transmission-gates should be constructed by both PMOS and NMOS to avoid degradation of data transfer characteristics caused by single-channel MOS usage. Therefore, instead of transmission-gate type circuit, we start with a combinational type circuit as shown in Fig. 6. To reduce the transistor-count based on logical equivalence, we consider a method consisting of the following two steps. As the first step, we plan to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals. Then, merge those parts in transistor level as the second step.

IV. PROPOSED TOPOLOGICALLY COMPRESSED FLIP -FLOP

A. Proposed FF and Transistor Level Compression.

After investigating many kinds of latch circuits, we have setup an unconventionally structured FF, shown in Fig. 7. This FF consists of different types of latches in the master and the slave parts. The slave-latch is a well-known Reset-Set (RS) type, but the master-latch is an asymmetrical single data input type. The feature of this circuit is that it operates in single phase clock, and it has two sets of logically equivalent input AND logic, X1 andY1, and X2 and Y2. Fig. 8 shows the transistor-level schematic of Fig. 7. Based on this schematic, logically equivalent transistors are merged as follows. For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 8 can be shared as shown in Fig. 9. When either N3 or CP is Low, the shared common node becomes VDD voltage level, and N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N3 and CP.As well as M1 and S1 blocks, two PMOS transistor pairs in M

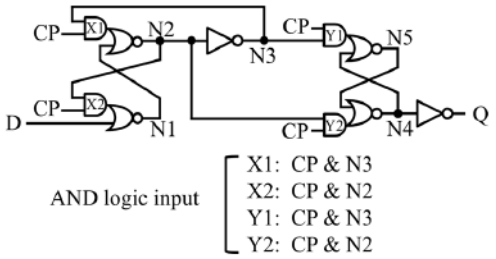


Figure 7: Schematic of Proposed Flip Flop

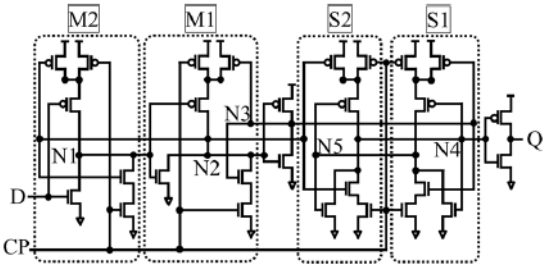


Figure 8: Transistor level Schematic of Proposed Flip Flop

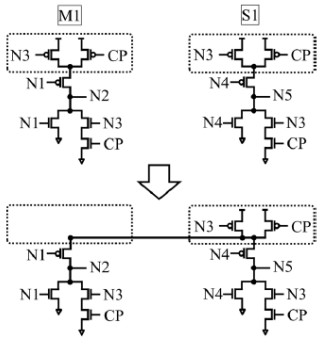


Figure 9: Transistor merging in PMOS side

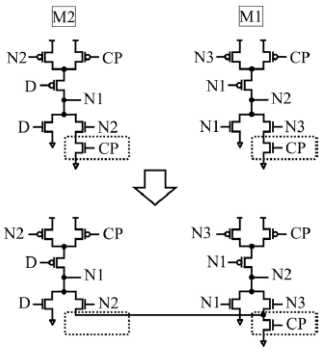


Figure 10: Transistor merging in NMOS side

And S2 blocks are shared. For the NMOS side, transistors of logically equivalent operation can be shared as well. Two transistors in M1 and M2 blocks in Fig. 10 can be shared. Transistors in S1 and S2 are shared as well.

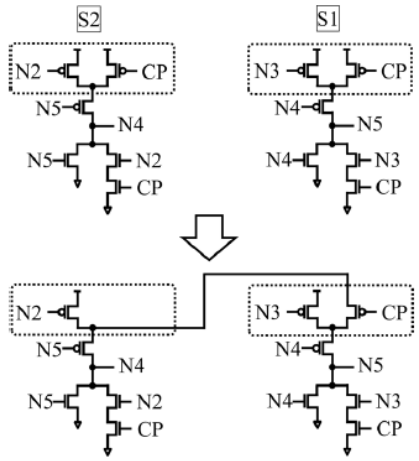


Figure 11: further transistor merging in PMOS side

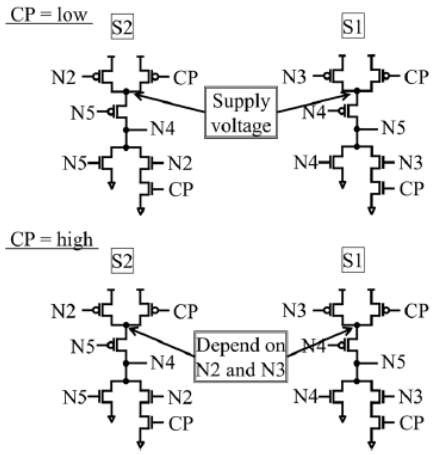


Figure 12: The state of internal nodes

Further in the PMOS side, CP-input transistors in S1 and S2, shown in Fig. 11, can be merged, because N2 and N3 are logically inverted to each other. When CP is Low, both nodes are in VDD voltage level, and either N2 or N3 is ON. When CP is High, each node is in independent voltage level as shown in Fig.12. In consideration of this behavior, the CP-input transistors are shared and connected as shown in Fig.11. The CP-input transistor is working as a switch to connect S1 and S2.This process leads to the circuit shown in Fig. 13. This circuit consists of seven fewer transistors than the original circuit shown in Fig. 8. The number of clock-related transistors is only three. Note that there is no dynamic circuit or pre-charge circuit, thus, no extra power dissipation emerges. We call this reduction method Topological Compression (TC) method. The FF, TC-Method applied, is called Topologically-Compressed Flip-Flop (TCFF).

B. Cell Operation

Fig. 14 shows simulation waveforms of the circuit shown in Fig. 13. In Fig. 13, when CP is low, the PMOS transistor connected to CP turns on and the master latch becomes the data input mode. Both VD1 and VD2 are pulled up to power-supply level, and the input data from D is stored in the master latch. When CP is high, the PMOS transistor connected to CP turns

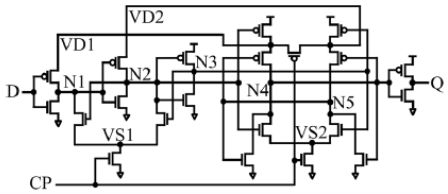


Figure 13: Transistor level schematic of topologically compressed flip-flop (TCFF)

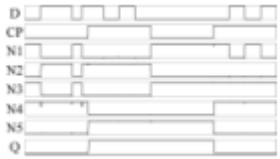


Figure14: wave form of simulation

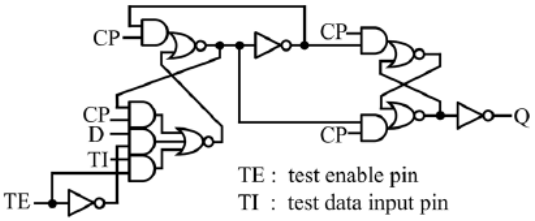


Figure 15: TCFF with scan type

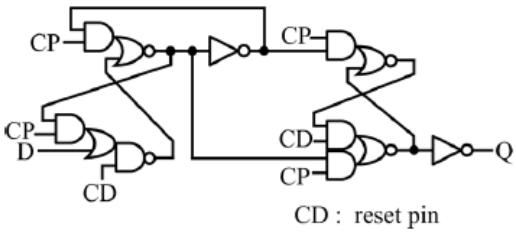


Figure 16: TCFF with reset type

off, the NMOS transistor connected to CP turns on, and the slave latch becomes the data output mode. In this condition, the data in the master latch is transferred to the slave latch, and then outputted to Q. In this operation, all nodes are fully static and full swing. The current from the power supply does not flow into the master and the slave latch simultaneously because the master latch and the slave

latch become active alternately. Therefore, timing degradation is small on cell performance even though many transistors are shared with no increase in transistor size.

C. Cell Variation

LSI designs require FFs having additional functions like scan, reset, and set. The performance and cell area for these cells are also important. TCFF easily realizes these cells with less transistor-count than conventional FFs. The circuit diagrams of TCFF with scan, reset, and set are shown in Figs.15-17 Each circuit can be designed with similar structure, and these FFs also have three transistors connected to CP so the power dissipation
is nearly the same as that of TCFF. Detailed characteristics are shown in Section V

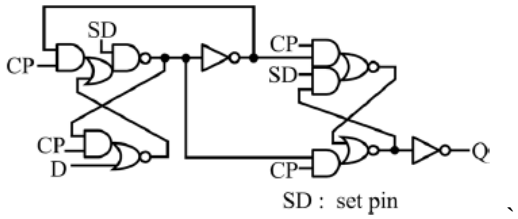
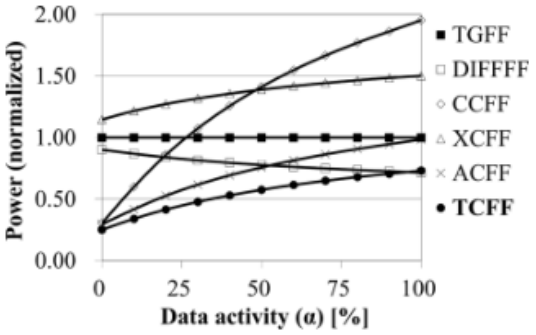


Figure 17: TCFF with set type



Process : 40 nm Temperature : 25˚C
Condition : typical Voltage : 1.1 v
Output capacitance : 10 fF
Data activity (α) : data transition probability

Fig. 18. Power simulation results of TCFF and other FFs.

V. PERFORMANCE SIMULATION

The performance of TCFF is demonstrated by SPICE simulation with 40 nm CMOS technology. For comparison with other FFs, the same transistor size is applied for every transistor in each FF including TCFF in order to simulate the same conditions. Some standard values are assumed for transistor sizes for the purpose of comparison; 0.24 m for width and 0.04 m for length in PMOS, and 0.12 m for width and 0.04 m for length in NMOS.

Fig.18 shows the normalized power dissipation versus data activity compared to other FFs. TCFF consumes the least power among them in almost all ranges of data activity. Average data activity of FFs in an LSI is typically between 5% and 15%. The power dissipation of TCFF is 66% lower than that of TGFF at 10% data activity. In the same way at 0% data activity, it is 75% lower. Table I summarizes the transistor-count, the CP-Q delay, the setup/hold time, and the power ratio of each FF. As for delay, TCFF is almost the same as the conventional FF, and better than other FFs. Setup time is the only inferior parameter to the conventional FF, and about 70 ps larger than the value of the conventional one. For hold time, TCFF is better than the conventional FF. In summary, only setup time is large, but TCFF keeps competitive performance to the conventional and other FFs.

Fig. 19 shows the supply-voltage dependence of the CP-Q delay. TCFF is possible to operate down to 0.6 V supply voltage due to essentially fully-static function. Though TCFF operates with single phase clock signal, a clock buffer is not necessary. The circuit is directly driven from a clock pin. Fig. 20 shows the clock-input-slew dependence of the CP-Q delay. ACFF

TABLE I
PERFORMANCE COMPARISON OF TCFF AND OTHER FFS

	#Tr.	CP-Q delay	setup	hold	power (α=10%)
TGFF	24	183	38	-15	1.00
DiffFF	22	209	-7	70	0.87
CCFF	42	225	173	-135	0.60
XCFF	21	221	-26	57	1.22
ACFF	22	176	139	-93	0.42
TCFF	21	176	105	-69	0.34

Process : 40 nm Temperature : 25 ˚C
Condition : typical Voltage : 1.1 v
Output capacitance : 10 fF
#Tr. : number of transistor in FF
CP-Q delay : average CP-to Q delay of D=high and low
setup and hold : defined at CP-to-Q delay increased 10% from stable value.
power : ratio normalized by TGFF
Unit of performance : ps

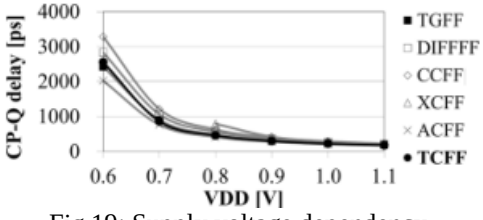
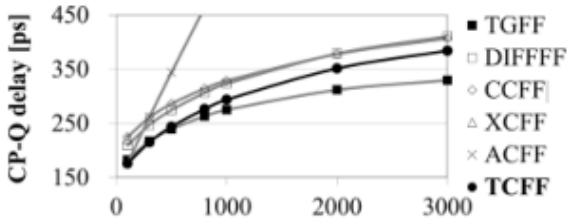


Fig 19: Supply voltage dependency



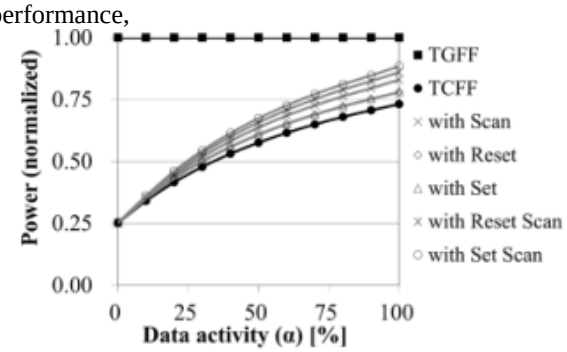
CP input slew variation

Fig 20: input slew dependency.

has more clock-input-slew dependence compared to other FFs, thus it becomes difficult to use in large input transition time.

The characteristics of TCFF are stable and the second best following TGFF.

Fig. 21 shows the normalized power versus the data activity for six varieties of TCFF including the basic type, and Table II shows performances of various TCFFs in the same conditions as Table I. Every cell inherits the strength of the original TCFF cell structure. No difference is observed among cell variations. Fig. 22 shows the layout of TGFF and TCFF with scan. Because TCFF needs more wiring resources for master and slave latch in the layout, it uses metal3 as compared to TGFF using up to metal2. But because the number of transistors in TCFF is fewer than the TGFFs, TCFF can be realized in slightly smaller cell area than the conventional one. In this layout, the area is adjusted to grid base design, resulting in the same area as the conventional one. Thus, it is easy to replace the conventional FF with TCFF if the cell replacement process is executed after pre-layout and timing analysis. In this section, TCFF's lowest power dissipation, competitive performance,



Process : 40 nm Temperature : 25˚C
Condition : typical Voltage : 1.1 v
Output capacitance : 10 fF
Data activity (α) : data transition probability per clock cycle
Power (normalized) : each FF normalized by TGFF

Fig 21: Power simulation results of various TCFFs

TABLE II
PERFORMANCE COMPARISONS OF VARIOUS TCFFS

	#Tr.	CP-Q delay	setup	hold	power (α=10%)
TCFF	21	176	105	-69	0.34
with Reset	25	183	111	-79	0.35
with Set	25	181	109	-63	0.35
with Scan	29	178	129	-97	0.35
with Reset Scan	33	185	148	-115	0.36
with Set Scan	33	183	136	-91	0.36

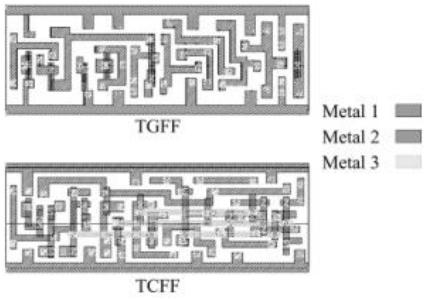


Fig22: The cell layout with scan.

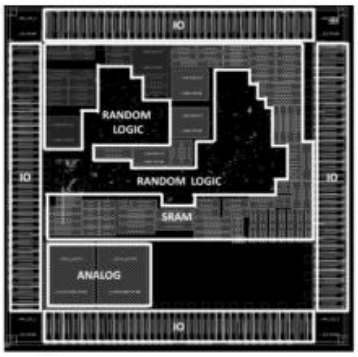
and cell area are explained. In the next section, how effectively TCFF is applied to actual chip design is shown by placement and routing experiment.

VI. EXPERIMENTAL CHIP LAYOUT

In order to estimate the effect when applying to a chip design, an experimental netlist is implemented in a 2 mm square chip by utilizing commercial logic synthesis and P&Rtool.Fig.23shows the layout and outline of the experimental chip. It consists of random logic, SRAM, analog, and I/O. The random logic consists of FFs, clock drivers, and other logic. In order to verify how TCFF is effectively applied to chip design, two types of front-end cell libraries are prepared. One is a conventional set with TGFF, and the other is a set including TCFF in addition to TGFF. Using these two libraries, logic synthesis and P&R are

TABLE III
EXPERIMENTAL CHIP LAYOUT DESIGN SUMMARY

K=1024		Original (TGFF only)			TGFF add TCFF		
		#Cell [K]	#Tr [K]	Area [mm²]	#Cell [K]	#Tr [K]	Area [mm²]
Design	TGFF	61.5	1850.9	0.228	1.3	43.3	0.005
	TCFF	-	-	-	60.2	1624.3	0.222
	Clock driver	1.5	22.8	0.003	1.4	22.2	0.003
	Other logic	278.7	2294.2	0.300	281.1	2364.5	0.308
Total		341.6	4167.9	0.530	344.0	4054.4	0.538
Ratio(vs Original)		1.0	1.0	1.0	1.007	0.973	1.013
Ratio of FF(#Tr)		0.44			0.41		
#Cell (TCFF/total FF)		-			0.98		



Process : 40 nm
Chip size : 2 mm × 2 mm
Cell variation : SRAM, Analog, I/O, Random logi
Clock frequency : 250 MHz
Number of gate in Random logic : 1M
Flip-flop in Random logic : 44 %

Fig 23: The experimental chip layout

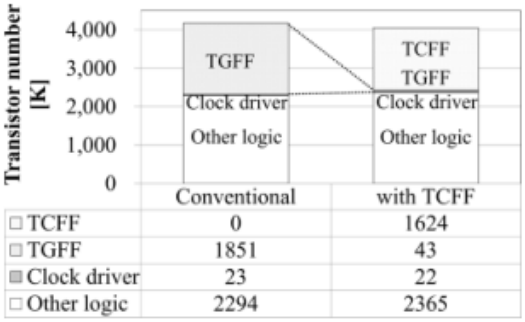


Fig24: Transistor count of random logic area with and without TCFF.

executed independently and those results are compared. In logic synthesis, the power-reduction option is highly applied. Fig. 24 and Table III show the logic synthesis and P&R results at 250 MHz clock frequency. After applying the library including TCFF, 98% of TGFF which occupy 44% of the random logic are replaced by TCFFs. Almost all TCFFs meet the timing constraints despite TCFF having larger setup time of 105 ps instead of 38 ps of TGFF as shown in Table I. As regards area size, only 1.3% increased with the TCFF-included library even though TCFF uses one more metal layer than TGFF in cell layout. This shows TCFF has no disadvantage in P&R process.

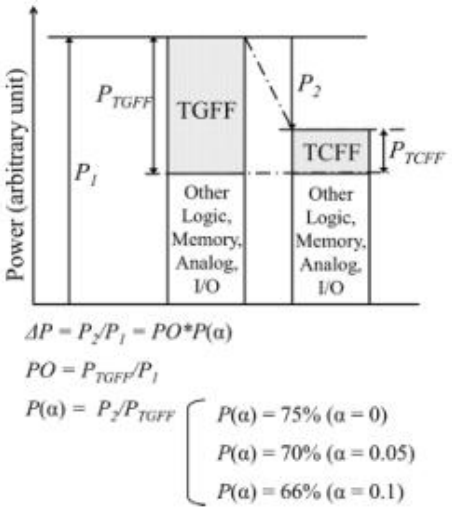


Fig25: Power reduction estimation in a chip

From these results, it is shown that the TCFF can easily replace TGFF while keeping timing performance and almost the same area size.

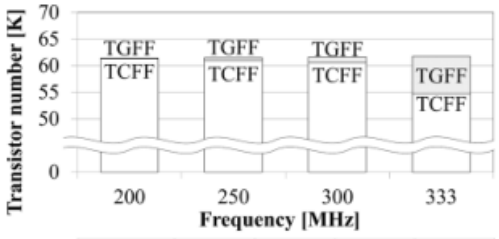
As regards total chip-level power reduction rate, it strongly depends on the application. In general, the power reduction effect by introducing TCFF is estimated by the following formula (see Fig. 25):

$$\Delta P = PO * RP * P(\alpha)$$

Where ΔP is chip power reduction ratio, *PO* is FF occupation ratio, *RP* is replacement rate, and $P(\alpha)$ is power reduction ratio of FF with data activity (α). In the experimental chip layout, FF occupation ratio in random logic is 44%, is 98%, and (10%) is 66%. Therefore, assuming the ratio of random logic power to the whole chip is 60%,17% chip power reduction ratio (ΔP) is expected.

VII. COUNTERMEASURE TO VARIOUS SPEED SYSTEMS

In Section VI, we investigated the effect when applying to a250 MHz system design in 40 nm CMOS technology. In this section, we show how effectively TCFF is applied to various systems especially to a higher speed case in terms of power and performance. Fig. 26 shows the result about replacement rate of TGFF to TCFF in various clock frequencies. The same front-end cell libraries and netlists as Section VI are used, and only clock cycle condition is set up from 200 MHz to 333 MHz



TGFF [%]	0.19	0.82	1.79	11.41
TCFF [%]	99.81	99.18	98.21	88.59

Fig26: Freequency dependent of replacement from TGFF to TCFF

TABLE IV
PERFORMANCE OF TGFF, TCFF AND RESIZED TCFF.

	CP-Q delay	setup	hold	power (α=10%)
TGFF	183	38	-15	1.00
TCFF	176	105	-69	0.34
TCFF resized	167	83	-57	0.47

power : ratio normalized by TGFF
Unit of performance : ps

as a parameter. In the condition from 200 MHz to 300 MHz, more than 98% of TGFF are replaced to TCFF. However, in caseof333MHzcondition, replacement rate goes downto88%, probably because of setup timing issue. Finally, at 360 MHz the timing constraint is not satisfied even if TGFFs are fully used.

In order to use TCFF around the critical condition, adjustment of transistor size is considered. In TCFF, since data-input or data-output operation is controlled by three clock-related transistors, by changing the size of those transistors, performance can be changed. Changing only three transistors in 21 transistors of a TCFF circuit does not affect cell area much. Table IV shows performance of TGFF, TCFF, and the resized TCFF. In the resized TCFF, only the three clock-related transistors are doubled in size.Fig.27 shows the normalized power dissipation for TCFF and the resized TCFF compared to TGFF. Compared to the original TCFF, delay and setup time is improved by 5% and 21%, respectively, in the resized TCFF. Power dissipation increases 39%, but is still 53% lower than TGFF. Fig. 28 shows the result of replacement in 333 MHz clock frequency including the resized TCFF in addition to TGFF and the original TCFF. Total replacement rate is as much as 95%, and 88% is replaced by the original TCFF and 7% is replaced by the resized TCFF. In summary, including a variety of clock-related transistor sizes, TCFF can be applied to various speed systems, and it can reduce whole chip power more effectively.

VIII. C ONCLUSION

An extremely low-power FF, TCFF, is proposed with topological compression design methodology. TCFF has the lowest power dissipation in almost all range of the data activity compared with other low-power FFs. The power dissipation of TCFF is 75% lower than that of TGFF at 0% data activity without area overhead. The topology of TCFF is easily expandable to various kinds of FFs without performance penalty. Applying to a 250 MHz experimental chip design with 40 nm

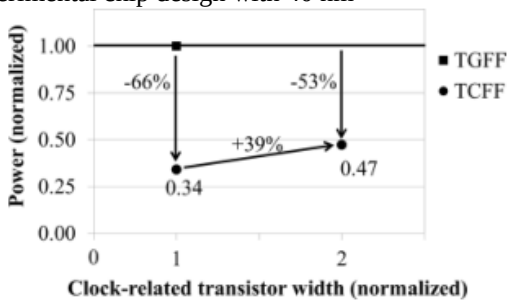


Fig 27: Power dissipation for TCFF and the resized TCFF.

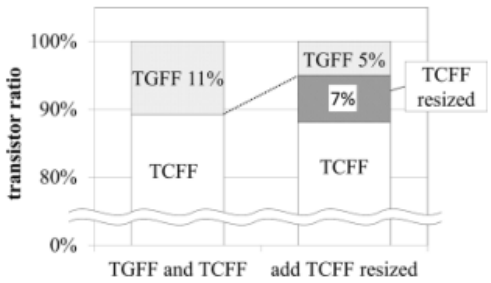


Fig. 28. Frequency dependence of replacement from TGFF to TCFF and the resized TCFF.

CMOS technology, 98% of conventional FFs are replaced by TCFFs. In a whole chip, 17% power reduction is estimated with little overhead of area and timing performance.

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